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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/646,681	08/21/2003	Ryan Lei	42P16687	1018

8791 7590 04/06/2005

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EXAMINER	
ISAAC, STANETTA D	

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 04/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/646,681	LEI ET AL.	
	Examiner	Art Unit	
	Stanetta D. Isaac	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 January 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) *2,6,13,26,31 and 32* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,4,5,7-12,14-25 and 27-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

LYNNE A. GURLEY
PRIMARY PATENT EXAMINER
TC 2800, AU 2812

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8/21/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the election filed on 1/07/05. Currently, claims 1-32 are pending.

Election/Restrictions

Applicant's election of claims 1-30 (drawn to method), and claims 1, 3-5, 7-12, 14-25 and 27-30 (drawn to Species I, figures 1A-1E), in the replies filed on 9/28/04 and 1/7/05, respectively, are acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction and species requirements, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Claims 2, 6, 13, 26, 31 and 32 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected species, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 1/7/05.

Information Disclosure Statement

The information disclosure statement (IDS) was submitted on 8/21/03. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Specification

The disclosure is objected to because of the following informalities: On page 7, paragraph [0022], line 8, "CVP" should be spelled "CVD". Appropriate correction is required.

The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 5, 8, 16-18 and 29 recites the limitation "...through the first dielectric film to define a cleaving plane." in line 2, of claims 5, 15 and 29, respectively. There is insufficient antecedent basis for this limitation in the claim. Specifically, on page 17, paragraphs [0050-0051], the disclosure of the ion implantation step through the first dielectric film to define a cleaving plane, are drawn to the non-elected Species III (figures 3A-3F).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 3, 5, 7-12, 14, 16-25, 27, 29 and 30 are rejected under 35 U.S.C. 102(e) as being anticipated by Yonehara International Publication Number WO 2004/100268.

Yonehara discloses the semiconductor method as claimed. See figures 1-9, and corresponding text, where Yonehara teaches, pertaining to claims 1, 12 and 22, a method of forming a germanium-on-insulator (GOI) substrate comprising: forming an epitaxial germanium layer **13** on top of a first substrate **11** (the epitaxial germanium layer having a rough surface, the rough surface has a roughness value approximately greater than 2nm RMS, for claim 12; figure 3; page 5, lines 21-25, ***Note***: the Examiner takes the position that it is inherent the rough surface has a roughness value approximately greater than 2nm RMS, based on Applicant's admitted prior art on page 6, paragraph [0019]); forming a first dielectric film **14** on top of the epitaxial germanium layer (on top of the rough surface, for claim 12; figure 4; page 6, lines 17-27); providing a second substrate **20** (figure 5; page 7, lines 1-3); bonding the first substrate to the second substrate by bonding the first dielectric film to the second substrate, the bonding resulted in a bonded wafer pair **30** (figure 5; page 7, lines 1-8); and removing the first substrate after the bonding to expose epitaxial germanium layer to form the GOI substrate **40** (and forming an electronic device on the GOI substrate, for claim 22; figures 6-9; page 7, lines 9-27; page 8, lines 1-15; page 17, lines 7-24).

Pertaining to claims 3, 14 and 27, Yonehara teaches, a method, wherein the removing of the first substrate after the bonding includes one of a grind back process, an etching process, and an ion exfoliation process (page 7, lines 9-24).

Pertaining to claims 5, 16 and 29, Yonehara teaches, a method further comprises causing an ion implantation to the first substrate through the first dielectric film to define cleaving plane (page 7, lines 9-24).

Pertaining to claims 7, 17 and 30, Yonehara teaches, a method wherein the removing of the first substrate after the bonding includes cleaving off the first substrate (page 7, lines 9-24).

Pertaining to claims 8 and 18, Yonehara teaches, a method further comprising: polishing the surface of the first dielectric film after the ion implantation, the polishing performs at least one of providing a smooth surface for the first dielectric film, repairing surface damages on the first dielectric film, and providing a clean surface for bonding (page 7, lines 9-24).

Pertaining to claims 9 and 19, Yonehara teaches, a method wherein each of the first substrate and the second substrate semiconductor wafer is selected from a group consisting of a silicon (Si) substrate, a monocrystalline Si substrate, a polycrystalline Si substrate, a Si-containing substrate, a Si substrate having an oxide layer, a silicon-on-insulator (SOI) substrate, a gallium arsenide substrate, and Ge-containing substrate (page 5, lines 10-11).

Pertaining to claims 10 and 20, Yonehara teaches, a method further comprising causing a surface activation to the top surface of the first dielectric film and at least one surface of the second substrate to facilitate the bonding (figure 5; page 7, lines 1-8).

Pertaining to claims 11 and 21, Yonehara teaches, a method further comprises annealing the bonded wafer pair at a predetermined annealing temperature, wherein the annealing temperature is achieved with a temperature ramp rate of approximately 1°C/minute (page 11, lines 18-24).

Pertaining to claim 23, Yonehara teaches, a method wherein the electronic device includes one of a transistor and a detector (page 17, lines 21-24).

Pertaining to claim 24, Yonehara teaches, a method wherein the transistor includes a gate dielectric, a gate electrode, spacers, and source/drain regions (page 17, lines 21-24, ***Note***: the Examiner takes the position that it is inherent that a spacers are included since it is conventionally well known that transistors include sidewall spacers).

Pertaining to claim 25, Yonehara teaches, a method wherein the detector includes a waveguide encapsulated by an oxide layer and at least one electrode (page 17, lines 21-24, ***Note***: the Examiner takes the position that it is inherent that a detector device is included since Yonehara teaches that other semiconductor devices can be formed).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 4, 15 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yonehara International Publication Number WO 2004/100268 in view of admitted prior art.

Yonehara discloses the semiconductor method substantially as claimed. See preceding rejection of claims 1, 3, 5, 7-12, 14, 16-25, 27, 29 and 30 under 35 U.S.C. 102(e).

However, Yonehara fails to show, pertaining to claims 4, 15 and 28, a method, further comprising: polishing the surface of the first dielectric film prior to the bonding.

On page 8, paragraph [0025], the Applicant teaches, that portions of the dielectric layer, can be removed to have a smaller thickness, where a conventional method of chemical mechanical polishing (CMP) may be used to remove some of the dielectric layer.

It would have been obvious to one of ordinary skill in the art to incorporate, a method further comprising: polishing the surface of the first dielectric film prior to the bonding, in the method of Yonehara, pertaining to claims 4, 15 and 28, according to the teachings of the admitted prior art, with the motivation of, reducing the amount of dielectric material, for the purpose of creating a desired dielectric thickness.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stanetta D. Isaac whose telephone number is 571-272-1671. The examiner can normally be reached on Monday-Friday 9:30am -6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Lebentritt can be reached on 571-272-1873. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Stanetta Isaac
Patent Examiner
March 28, 2005

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